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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/963,533	ARAI, TAKAO
	Examiner	Art Unit
	Johannes P Mondt	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-14 and 27-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 8-14 and 27-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment B filed 02/19/03 and entered as Paper No. 7 forms the basis of this office action. In Amendment B, Applicant amended the specification and claims 2, 5, 11 and 12, canceled claims 6-7 and newly added claims 27-40. Comments to Remarks in said Amendment B found under "Response to Arguments" are thus restricted to those aspects requiring clarification of the original rejection of the original claim still pertinent to the new claim set.

Response to Arguments

Remarks in Amendment B have been fully considered but are not persuasive. In particular, although the amendment to the specification is acceptable and the rejection under 35 USC 112, second paragraph, of claim 5 for lack of antecedent basis can be removed in light of Amendment B, the traverse of the art rejections based on Aoki et al can not be accepted, because:

(a) counter to Applicant's allegation on page 11 (final full paragraph), the channel region 2B has an impurity type different from that in the substrate 1 (cf. column 2, lines 34-36; also see the Figure illustrating said channel region 2B);

(b) region 2B inherently insulates the channel region 2A from the gate (as otherwise the charge carriers would not form said channel in region 2A but rather in region 2B), and is enabled to perform an insulating function because of its extremely low impurity concentration ($10^{13}\,cm^{-3}$) (cf. column 2, lines 31-48), for which the semiconductor is an insulator (see, for instance, S.M. Sze, "Physics of Semiconductor

Devices", second edition, John Wiley (New York, 1981), specifically page 32 and Figure 21, showing the resistivity for 10^{13} cm^{-3} to be up by more than four decades from that in the substrate (10^{17} cm^{-3}), namely: at least 3 KOhm . cm instead of less than 0.1 Ohm.cm. Therefore, region 2B is a gate insulating film, while region 2A is a channel region of a first conductivity type being selectively provided in a semiconductor region of second conductivity type", counter to Applicant's allegation on pages 11-12 of Remarks in said Amendment B. See also claim 4 in Aoki et al.

(c) counter to Applicant's allegation on page 12, second full paragraph, said channel region in region 2A is provided in a semiconductor region of second conductivity type, because region 2A is (buried) in the semiconductor substrate 1. Pertinent in this regard is the material and topological properties (rather than the method of making), which as claimed did not distinguish from those in Aoki et al; see for instance Applicant's disclosure in which the channel region 6 (e.g., Figures 2), is positioned in exactly the same manner relative to its substrate as region 2A relative to its substrate in Aoki et al.

(d) Because an upper level of said substrate as actually referred to by the examiner are at least, comprising of the upper surfaces of the ion implantation regions (see, for instance, regions 3 and 4 in Figure 1 and regions 5 in Figure 5 in Aoki et al), the channel is clearly positioned lower than an upper surface of said substrate.

With regard to the traverse (page 14 of Remarks) of the rejection under 102(e) as anticipated by the embodiment of Figure 5 in Aoki et al, the same arguments apply as above, because the channel region here is only separated from the substrate by virtue

of the formation of the actual channel, whilst the channel itself has to be of the same conductivity type as the abutting source and drain regions 5, the latter being of opposite conductivity type as that of the substrate 1. Finally, the presence of an additional gate insulating film in the form of a gate oxide layer in Aoki et al is allowed, considering the claim language of Applicant: a composite gate insulating film is still a gate insulating film.

For the above reasons the traverse of the rejection under 102(e) as anticipated by Aoki et al is maintained.

With regard to the traverse of the rejection of claim 8: arguments by Applicant are comprised entirely of arguments made in connection with claim 1 and have already been addressed above.

Claim 11 has been substantially amended and thus needs not to be commented upon.

The art rejections included below are based on the above considerations and on the findings of the prior art found for the substantially amended or newly introduced claims.

Claim Objections

1. ***Claim 11*** is objected to because of the following informalities: "an impurity diffused region of a first conductivity type" (lines 2-3) should be replaced by "an impurity diffused region of a first conductivity type comprising a channel region". Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. ***Claims 11-14*** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, claim 11 as amended contains a first phrase "an upper surface of the semiconductor region being exposed at an upper surface of said semiconductor wafer on each end of the oxide film". However, this first phase implies that there is an upper surface at both ends rather than the single upper surface implied by the quoted first phrase and by a second phrase "at a lower level than the upper surface" following said first phrase. Claims 12-14 are equally rejected because of their dependence on claim 11.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. ***Claims 1, 3, 8, 10, 30-31*** are rejected under 35 U.S.C. 102(e) as being anticipated by Aoki et al (6,229,188 B1).

Aoki et al (cf. Figures 1 and 5) teach a channel region (the region underneath 9 in Figure 5, see column 3, lines 8-10; region 2A in Figure 1, see column 2, lines 30-31)

of a depletion type lateral field effect transistor (see claim 1 of Aoki et al, column 4, lines 28-34), said channel region (region 2A for Figure 1: cf. column 2, lines 20-40, and epitaxial doped region 9 in Figures 5: cf. column 3, line 30) of first conductivity type being selectively provided in a semiconductor region 1 of second conductivity type (cf. column 2, lines 20-40), and said channel region underlying a gate insulating film (region 10 in Figure 5, regions 2B and 5 in Figure 1), wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region (cf. column 2, lines 30-31). In conclusion, Aoki et al anticipate claim 1.

With regard to claim 3: in view of claim 1 the channel region is of first conductivity type, while whether this conductivity type is achieved by diffusion or by ion implantation is irrelevant to the device but instead pertains to aspects of method of making the device; while it is inherent to the doping concentration of said channel region to be used for a threshold voltage adjustment if needed. The further limitation of claim 3 is thus seen not to distinguish over the prior art.

With regard to claim 8: Aoki et al teach (cf. Figures 1 and 5) a depletion type lateral MOS field effect transistor comprising: a channel region (2A in Figure 1 and region underneath gate oxide region 10 in Figures 5, region 9 in Figures 5) of first conductivity type being selectively provided (by doping) in a semiconductor region of second conductivity type (cf. column 2, lines 20-40 and column 3, lines 5-40); source and drain regions of first conductivity type being selectively provided in said semiconductor region (regions 3 and 4 in Figure 1, regions 5 in Figures 5), said channel

region being interposed between said source and drain regions (inherent in lateral MOSFET); a gate insulating film (5 in Figure 1, 10 in Figures 5) extending over said channel region; and a gate electrode (6 in Figure 1, 11 in Figures 5) provided on said gate insulating film, wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region.

With regard to claim 10: in view of claim 8 the channel region is of first conductivity type, while whether this conductivity type is achieved by diffusion or by ion implantation is irrelevant to the device but instead pertains to aspects of method of making the device; while it is inherent to the doping concentration of said channel region to be used for a threshold voltage adjustment if needed. The further limitation of claim 10 is thus seen not to distinguish over the prior art.

With regard to claims 30-31: the depletion layer lateral MOSFET by Aoki et al has a channel region 2A provided in the semiconductor region 1, said channel region comprising, throughout the channel region, both types of free carriers, i.e., both electrons and holes, by dint of the statistical equilibrium between said two types of free carriers, while the channel region is itself of first conductivity type, which is n-type, i.e., by necessity the same as that of source and drain in a depletion-type lateral field effect transistor (claim 1) or depletion-type lateral MOSFET (claim 8), as already contained as respective limitations in claims 1 and 8 on which claims 31 and 30 respectively depend. Furthermore, the semiconductor region comprises a third concentration of first impurities of the second conductivity type (p-type), said third concentration being higher than the first concentration (cf. column 2, lines 32-34).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 11-13*** are rejected under 35 U.S.C. 102(b) as being anticipated by Sase (JP406021451A). Sase teaches a semiconductor wafer including:

an impurity diffused region of first conductivity type (the MOS is an NMOS device: see [0009]) comprising a channel region (numeral 304 in Figure 3(c); see [0011]) being selectively provided in a semiconductor region of a second conductivity type (p-type) (cf. numeral 300 in Figure 3(a): see [0010]); and

an oxide film (numeral 303 in Figure 3(c): see [0011]) overlying said impurity diffused region 304 with an upper surface of the semiconductor region 300 being exposed at an upper surface of said semiconductor wafer on each end of the oxide film (see Figure 3(f)),

wherein an interface of said impurity diffused region 304 to said oxide film 303 lies at a lower level than the upper surface of said semiconductor wafer (see Figure 3(f)).

In conclusion, Sase anticipates claim 11.

With regard to claim 12: Sase teaches also a CMOS application of his invention (cf. [0018]; his invention is in part motivated by the impossibility to apply the conventional art to a CMOS device, as explained in [0018]), which inherently involves one of the CMOS devices to be in a well of the same conductivity type as the underlying substrate. Therefore, Sase anticipates claim 12.

With regard to claim 13: in view of claim 11 the channel region is of first conductivity type, while whether this conductivity type is achieved by diffusion or by ion

implantation is irrelevant to the device but instead pertains to aspects of method of making the device; while it is inherent to the doping concentration of said channel region to be used for a threshold voltage adjustment if needed. The further limitation of claim 13 is thus seen not to distinguish over the prior art.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 2, 4, 12, 27, 32, 38-40*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al (6,229,188 B1) in view of Vo et al (5,424,226).

With regard to claims 2 and 12: As detailed above, claims 1 and 11 are anticipated by Aoki et al. Aoki et al do not necessarily teach the further limitation of claims 2 casu quo claim 12, however, it would have been obvious to include the teaching of said further limitation in view of Vo et al,, who teach a depletion-mode NMOS within a CMOS device requiring the inclusion of a well (inherent in the CMOS concept; see column 1, lines 48-60).

Motivation for including the teaching in this regard by Vo et al is the application of the invention by Aoki et al (improved threshold voltage determination) to the field of input noise reduction circuits (cf. column 1, lines 10-18). *Combination* of the inventions

is easily accomplished, as the presence of a well within the substrate, in which the channel resides, in no way affects the manufacturing process of the buried channel aspects. *Success* in implementing the combination can therefore be reasonably expected.

With regard to claim 4: as is the case in CMOS devices, said well region as introduced in the invention of Aoki et al by implementing the teaching by Vo et al plays the role of the substrate underlying the channel region (see also, for instance, Wolf, ISBN 0-961672-4-5; pages 383-389) and therefore has a conductivity type opposite the first conductivity type of the channel region for this depletion-mode device, while, as discussed above, according to the teaching of Aoki et al said well region having an upper surface and including an impurity-doped region selectively provided in said well region, said impurity-doped region being doped with an impurity of first conductivity type (namely: opposite the conductivity type of the well region), which impurity-doped region inherently can be used for adjusting the threshold voltage of said depletion type lateral field effect transistor, wherein said upper surface of said impurity-doped region lies at a lower level than said upper surface of said well region. Whether the impurity doping is achieved through diffusion or some other method such as ion implantation is irrelevant for the present device claim.

With regard to claim 27: said impurity diffused region as essentially taught by Aoki is a channel layer of a depletion type lateral field effect transistor (cf. claim 1 in Aoki et al).

With regard to claim 32: the depletion layer lateral MOSFET by Aoki et al has a channel region 2A provided in the semiconductor region 1, said channel region comprising, throughout the channel region, both types of free carriers, i.e., both electrons and holes, by dint of the statistical equilibrium between said two types of free carriers, while the channel region is itself of first conductivity type, which is n-type, i.e., by necessity the same as that of source and drain in a depletion-type lateral field effect transistor (claim 4), as already contained as a limitation in claim 4 on which claim 32 depends. Furthermore, the semiconductor region comprises a third concentration of first impurities of the second conductivity type (p-type), said third concentration being higher than the first concentration (cf. column 2, lines 32-34).

With regard to claims 38-40: As detailed above, claims 2, 4 and 12 are unpatentable over Aoki et al in view of Vo et al. Furthermore, Vo et al teach the distance "d" can be negative, in which case the well extends in a planar fashion over the entire length of the device (cf. column 1, line 68 and column 2, line 1), in which case, comprised in the teaching by Vo et al, the two wells overlap and form a planar well over the entire length of the device, in which case the devices will operate in depletion mode (cf. column 1, lines 53-60).

Motivation from adopting the teaching in this regard by Vo et al within the invention by Aoki et al stems from the circumstance that it the only consistent choice for "d" for the application of the teaching by Vo et al to the invention by Aoki et al to do so, since the device by Aoki et al is a depletion-type lateral MOSFET.

Motivation to include this teaching by Vo et al is, furthermore, to provide the correct threshold voltage for depletion type lateral MOSFET as taught by Aoki et al. *Combination* of the teaching with the invention is straightforward through an appropriate choice of n-well implantation (cf. column 2, lines 50-64). *Success* of the implementation of said combination can therefore be reasonably expected.

2. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al and Vo et al as applied to claim 4 above, and further in view of Sase (JP406021451A). As detailed above, claim 5 is unpatentable over Aoki et al in view of Vo et al. Neither Aoki et al nor Vo et al necessarily teach the further limitation of claim 5. However, as shown by Sase, for the specific purpose of simplifying the manufacturing process of a buried-channel MOSFET (cf. English abstract, "Purpose"), the impurity diffused region may be manufactured to abut the gate oxide region above it, by creating the buried channel through ion implantation within it, rather than through consecutive epitaxy (cf. fourth sentence of English abstract, "Constitution").

Motivation to include the teaching by Sase into the invention essentially taught by Aoki et al is to simplify the method of making, as explained by Sase (loc.cit. on purpose). *Combination* of said teaching with said invention is straightforward, considering the standard practice of ion implantation as a means to create strongly doped buried levels, because the typical ion implantation profile has a maximum for the ion concentration at finite depth, which can be adjusted to achieve the appropriate

positioning of the buried channel. *Success* in the implementation of said combination can therefore be reasonably expected.

3. ***Claim 9*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al in view of Vo et al (5,424,226) and Wolf (ISBN 0-961672-4-5). As detailed above, Aoki et al anticipate claim 8. Aoki et al do not necessarily teach the further limitation of claim 9; however, it would have been obvious to teach the channel region of claim 8 wherein said semiconductor region comprises a well region selectively provided in an epitaxial layer of first conductivity type overlying the semiconductor substrate of first conductivity type, because depletion-mode CMOS devices form an obvious field of application for the invention of Aoki et al in view of the advantages of depletion mode CMOS devices as taught by Vo et al (see column 1, lines 10-18), while for the purpose of reliability at the sub-micron level twin-well CMOS devices are advantageous (see Wolf, page 388) and said wells are usually built on epitaxial substrates for the suppression of latchup in CMOS (see Wolf, page 385).

4. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sase (JP406021451A in view of Aoki et al (6,229,188). As detailed above, Sase anticipates claim 11 (on which claim 14 depends). Sase does not necessarily teach the further limitation as defined by claim 14. However, the range that forms the essence of claim 14 overlaps that found in the prior art of the same device, i.e., a buried-channel MOSFET, as witnessed by Aoki et al who teach oxide film 2 to have a thickness of 6,000 Å (cf.

column 3, lines 5-12), although said thickness is reduced to about 3,000 Å immediately and vertically above said channel region. Applicant is reminded that a prima facie case of obviousness typically exists when the ranges of a claimed composition overlaps the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). In the underlying case, a thickness of 3,000 Å would not be expected to have essentially different properties than one of 5,000 Å, because the electric field caused by a gate voltage applied to a gate immediately above said oxide is not necessarily affected by the thickness of said oxide layer as much as it is by the specific constitution of said oxide layer, through its dielectric constant influencing the capacitance across it.

5. ***Claims 28-29*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sase (JP406021451A) in view of Wolf (ISBN: 961672-4-5) and Coe (4,939,390). Sase teaches a semiconductor substrate of first conductivity type; an impurity diffused channel selectively provided in said semiconductor substrate, said impurity diffused channel region being doped with an impurity of first conductivity type (cf. [0025]; boron ion implantation causes a P-type conductivity, which is the same conductivity type as the substrate's; see description of region 300 on page 8 of Sase), which inherently is for adjustment to a threshold voltage requirement of a lateral field effect transistor (the device of Sase is lateral because 107/108 are the source and drain regions (cf. English

abstract, "Constitution"), wherein said upper surface of said impurity diffused channel lies at a lower level than said upper surface of said semiconductor substrate.

Sase also explicitly teach and advocate the *application of his invention to CMOS* devices, in which *the existence of a well within the semiconductor substrate and of second conductivity type is inherent* (see [0018]).

Sase does not necessarily teach the further limitations (a) of an *epitaxial layer of first conductivity type* overlying said semiconductor substrate, and (b) application to a field effect transistor of the *depletion* type. However, ad (a), as shown by Wolf (pages 414-415) it is text book knowledge that it is advantageous to include an epitaxial layer of the same conductivity type as said semiconductor substrate in CMOS devices (i.e., of the devices which Sase advocates application of his invention to according to [0018]) so as to combat latchup, whilst the choice between depletion and enhancement type lateral field effect transistors is governed by the consideration whether one would like to have the transistor OFF or ON with the gate is OFF, as discussed by Wolf (pages 300-301).

Motivation to include the teaching ad (a) by Wolf in the invention as taught by Sase is the ubiquitous risk of latchup in CMOS devices (see Wolf, page 400); *motivation* to include the teaching ad (b) by Wolf in the invention by Sase is present in applications in which the device should be mostly in the ON state, in which case no gate voltage need to be applied most of the time, while, as explained by Coe, the depletion-mode device can be made at a smaller scale, thus decreasing parasitic capacitance (cf. column 6, lines 47-56), which, parenthetically also helps further reducing latchup problems (cf. Wolf, page 400). *Combination* of teachings (a) and (b) with the invention

as taught by Sase is straightforward as all that is required is to change the conductivity type of the source and drain regions to become of the same rather than opposite conductivity type as the impurity diffused region comprising the channel region. Impurity doping through ion implantation is standard in the art of field effect transistor processing. *Success* in implementing the invention can therefore be reasonably expected.

With regard to claim 29: In Sase, said upper surface of said impurity diffused region 304 is bounded with a gate insulating film 303 (see [0011]).

6. ***Claims 33-36*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sase (JP406021451A) in view of Wolf (ISBN: 961672-4-5) and Coe (4,939,390). Sase teaches a lateral field effect transistor, comprising a semiconductor substrate of first conductivity type with a first impurity concentration (cf. English abstract, and Figure 3(a), see definition of numeral 300 on page 8); an first conductivity type channel region 304 (cf. Figure 3c and definition on page 8) selectively provided in said semiconductor substrate, said impurity diffused channel region being doped with an impurity of first conductivity type (cf. [0025]; boron ion implantation causes a P-type conductivity, which is the same conductivity type as the substrate's; see description of region 300 on page 8 of Sase), which inherently is for adjustment to a threshold voltage requirement of a lateral field effect transistor (the device of Sase is lateral because 107/108 are the source and drain regions (cf. English abstract, "Constitution")), wherein an uppermost

surface of said channel region lies at a lower level than the uppermost surface of said semiconductor substrate.

Sase also explicitly teach and advocate the *application of his invention to CMOS* devices, in which *the existence of a well within the semiconductor substrate and of second conductivity type is inherent* (see [0018]).

Sase does not necessarily teach the further limitations (a) of an *epitaxial layer of first conductivity type* overlying said semiconductor substrate and of a concentration lower than that of the semiconductor substrate, and (b) application to a field effect transistor of the *depletion* type. However, ad (a), as shown by Wolf (pages 414-415) it is text book knowledge that it is advantageous to include an epitaxial layer of the same conductivity type as said semiconductor substrate in CMOS devices but lower in impurity concentration (i.e., of the devices which Sase advocates application of his invention to according to [0018]) so as to combat latchup, whilst the choice between depletion and enhancement type lateral field effect transistors is governed by the consideration whether one would like to have the transistor OFF or ON with the gate is OFF, as discussed by Wolf (pages 300-301). Finally, it is understood in the art of semiconductor devices, particularly field effect transistors, that a mere but overall and consistent interchange of all conductivity types does carry any patentable weight unless the specification explains why the particular choice of conductivity type is critical to the invention.

Motivation to include the teaching ad (a) by Wolf in the invention as taught by Sase is the ubiquitous risk of latchup in CMOS devices (see Wolf, page 400); *motivation*

to include the teaching ad (b) by Wolf in the invention by Sase is present in applications in which the device should be mostly in the ON state, in which case no gate voltage need to be applied most of the time, while, as explained by Coe, the depletion-mode device can be made at a smaller scale, thus decreasing parasitic capacitance (cf. Coe, column 6, lines 47-56), which, parenthetically also helps further reducing latchup problems (cf. Wolf, page 400). *Combination* of teachings (a) and (b) with the invention as taught by Sase is straightforward as all that is required is to change the conductivity type of the source and drain regions to become of the same rather than opposite conductivity type as the impurity diffused region comprising the channel region. Impurity doping through ion implantation is standard in the art of field effect transistor processing. *Success* in implementing the invention can therefore be reasonably expected.

With regard to claim 34: Sase teaches a gate oxide film (either 202 or 303) (cf. Figures 1a and 3c and definitions of 202 and 303 on page 8) extending over the channel region (cf. Figure 3c and moreover inherent in gate oxide film in lateral field effect transistors); field oxide films 201 contacting each end of the gate oxide film (cf. Figure 1a) and extending over the semiconductor substrate. Incorporation of the teachings by Wolf and Coe as delineated in the discussion of claim 33 (on which claim 34 depends) automatically has the gate oxide film extend over the p-well instead; a source region (204 and 306) contacting a first end of said channel region (said contact between source and channel is inherent for proper functioning of the channel), gate oxide film 303 and one of said field oxide films (field oxide films and gate oxide are

contiguous), and a drain region (204 and 306) contacting a second end of said channel region, gate oxide film and another of said field oxide films (cf. English abstract, "Constitution").

With regard to claim 35: Sase teaches the gate oxide 303 to extend over the channel region 304, whilst the channel region inherently contains both types of charge carriers, electrons and holes, whilst it contains more charge carriers of its conductivity type by virtue of the meaning of conductivity type, namely the type of free carriers that is in the majority. Therefore, the further limitation of claim 35 does not distinguish over the prior art as taught by Sase.

With regard to claim 36: Sase teaches the concentration of that part of the wafer (without the well this is the semiconductor substrate, see [0021]) that abuts the channel region to have a impurity concentration that is lower than that of the channel region 304 (cf. [0025]), namely $5x10^{16}$ for the semiconductor substrate and 3.3. x 10^{12} (cm^{-3}) for the channel region, while implementation of the well in view of Wolf according to the obvious argument given above in connexion with claim 33 implies that the well may be substituted for the semiconductor substrate in this regard. Therefore, the further limitation as defined by claim 36 is essentially taught by the primary reference and needs no further obviousness argument.

7. ***Claim 37*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sase (JP406021451A), Wolf (ISBN: 961672-4-5) and Coe (4,939,390) as applied to claim 34 above, and further in view of Burr et al (5,622,880). As detailed above, claim 34 is

unpatentable over Sase in view of Wolf and Coe. Sase teaches a gate oxide film of 15 nm = 150 Å thick (cf. [0023]), rather than twice this thickness as claimed in claim 37, while a specific thickness of the field oxide 201 is necessarily presented. However, as taught by Burr et al in a patent for a lateral MOSFET (cf. title), a range for the thickness of gate oxide 120 comprising a thickness of 65 Å and a range for the thickness of the field oxide 129 (cf. column 4, line 66) comprising a thickness overlapping with the range claimed by Applicant (thickness between *about* 2000 and 5000 Å) is known in the art Applicant, in his disclosure, does not explain why the claimed range for the gate oxide, consisting of a single value, is critical to the invention when juxtaposed both with the value of 65 Å taught by Burr et al and with the value of 150 Å as taught by the primary reference (Sase). Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
April 29, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800